AMENDMENTS TO THE SPECIFICATION:

Page 2:

Please substitute the following paragraph for the paragraph beginning at line 1:

In the existent NAND type flash memory, two active regions are connected, and are connected by way of contact holes to global bit lines, and first selection transistors for selecting two memory cell strings disposed in each of the active regions are arranged in two rows with gate wirings thereof being in parallel. The selection transistors in each row are constituted by serially connecting ~~an~~ enhancement type transistors and depletion type transistors alternately. Further, the source line is disposed in perpendicular to the active region, second selection transistors are disposed in one row so as to be connected with the source line, and a plurality of memory cell transistors each having a first gate and a second gate are connected in series between the first selection transistors in two rows and the second selection transistors in one row (for example, refer to Patent Document 1 infra).

Page 2:

Please substitute the following paragraph for the paragraph beginning at line 17:

Alternatively, there is a method of constituting selection transistors only with enhancement type transistors by separately disposing the first selection transistors and the second selection transistors, thereby saving ion implantation for forming depletion type transistors and thereby simplifying the production steps (for example, refer to Patent Document 2 infra).

Page 2:

Please substitute the following paragraph for the paragraph beginning at line 24:

In the two examples of the Patent Document 1 and the Patent Document 2 described above, two ~~roes~~rows of selection transistors and two contact holes necessary for connection of two ~~roes~~rows of the active regions with a common global bit line are simplified into selection transistors in two rows and one contact hole, thereby decreasing the area in the direction of bit line and reducing the chip area.

[Patent Document 1]

Page 9:

Please substitute the following paragraph for the paragraph beginning at line 10:

As shown in Fig. 1, on the active region 100, memory cell arrays each having a plurality of serial memory cells 101 are arranged in parallel by plural ~~row~~rows, to constitute a memory cell array MCA. A gate 102 of a selection transistor is disposed each by one on both ends of the memory cell rows, and gates of the selection transistors are separated on each of the active regions 100. Further, the gates of the selection transistors are disposed in two stages in the direction perpendicular to the global bit line 103 and the gate 102 of the selection transistor is disposed in each of the stages on every other active ~~regions~~region. Further, the gates 102 of the selection transistors are connected by way of contact holes 106 with a gate wiring 107 (refer to Fig. 1, Fig. 4 and Fig. 5).

Page 10:

Please substitute the following paragraph for the paragraph beginning at line 6:

A first selection transistor portion 104 and a second selection transistor portion 105 are disposed in two stages in the direction perpendicular to the global bit ~~lint~~line 103, and are disposed in mirror asymmetry with respect to the connection portion CNP of the active region 100

Page 12:

Please substitute the following paragraph for the paragraph beginning at line 6:

Further, the wirings ST1, ST2, ST2′ for the selection transistors are set to 0 V to turn OFF the selection transistors connected with the wirings. When the wiring ST1′ is set high to turn ON the selection transistors connected with the wiring row D and row D′ are selected and the potential on the global ~~bait~~bit line 103 is transferred to the row D and the row D'.

Page 17:

Please substitute the following paragraph for the paragraph beginning at line 20:

Then, Embodiment 6 of the nonvolatile semiconductor memory device according to the invention is to be described. This embodiment is an example of applying the invention to a nonvolatile semiconductor memory device of a constitution, in a layout capable of decreasing the size in the direction of the global bit line, having a third gate of different function in addition to first and second gates, in which the gate of the ~~select~~selection transistor is not separated on the active region. The nonvolatile semiconductor memory device having the third gate described above is disclosed, for example, in Patent Document 3.

Page 19:

Please substitute the following paragraph for the paragraph beginning at line 8:

The contact hole 108 is formed in each of the active regions of the first selection transistor portion 105 and ~~the~~ connected with the global bit line 103. 109 denotes a device isolation region comprising a silicon oxide film (field oxide film) and 115 denotes a gate wiring for the memory cell.

Page 20:

Please substitute the following paragraph for the paragraph beginning at line 1:

In this case, it may suffice that memory cell rows A, B, C, and D can be selected respectively by operating the first selection transistor portion 104 and the second selection transistor 105 in two stages. However, in the memory cell where the third gate different in the function from the first gate and the second gate is present being buried in a space between two first gates, since the source and drain diffusion layer is a virtual ground type using adjacent memory cell and the diffusion layer in common, adjacent row A and row A′ are operated as device isolation regions in a case of selecting, for example, a row B in Fig. 14, so that memory cell rows are selected on every ~~another~~other row.

Page 21:

Please substitute the following paragraph for the paragraph beginning at line 3:

On the other hand, when the wirings ST3′ and ST4′ are set to 0 V to turn OFF the ~~select~~selection transistor, and wiring ST3 is set to high to turn ON ~~select~~selection transistors, only the row B is selected and the potential on the source line is transferred to the row B. In this step, other memory cells are separated from the source line CS. In the same manner, row A is selected when the wiring ST4 is set high and other wirings are set to 0 V, row D is selected when wiring ST4′ is set high and other wirings are set to 0 V, row C is selected when wiring ST3′ is set high and other wirings are set to 0 V. Accordingly, in the memory cells where the two adjacent active regions are connected in common, row A′ is selected when the row A is selected, row B′ is selected when the row B is selected, row C′ is selected when the row C is selected, and row D′ is selected when the row D is selected.